

1/9

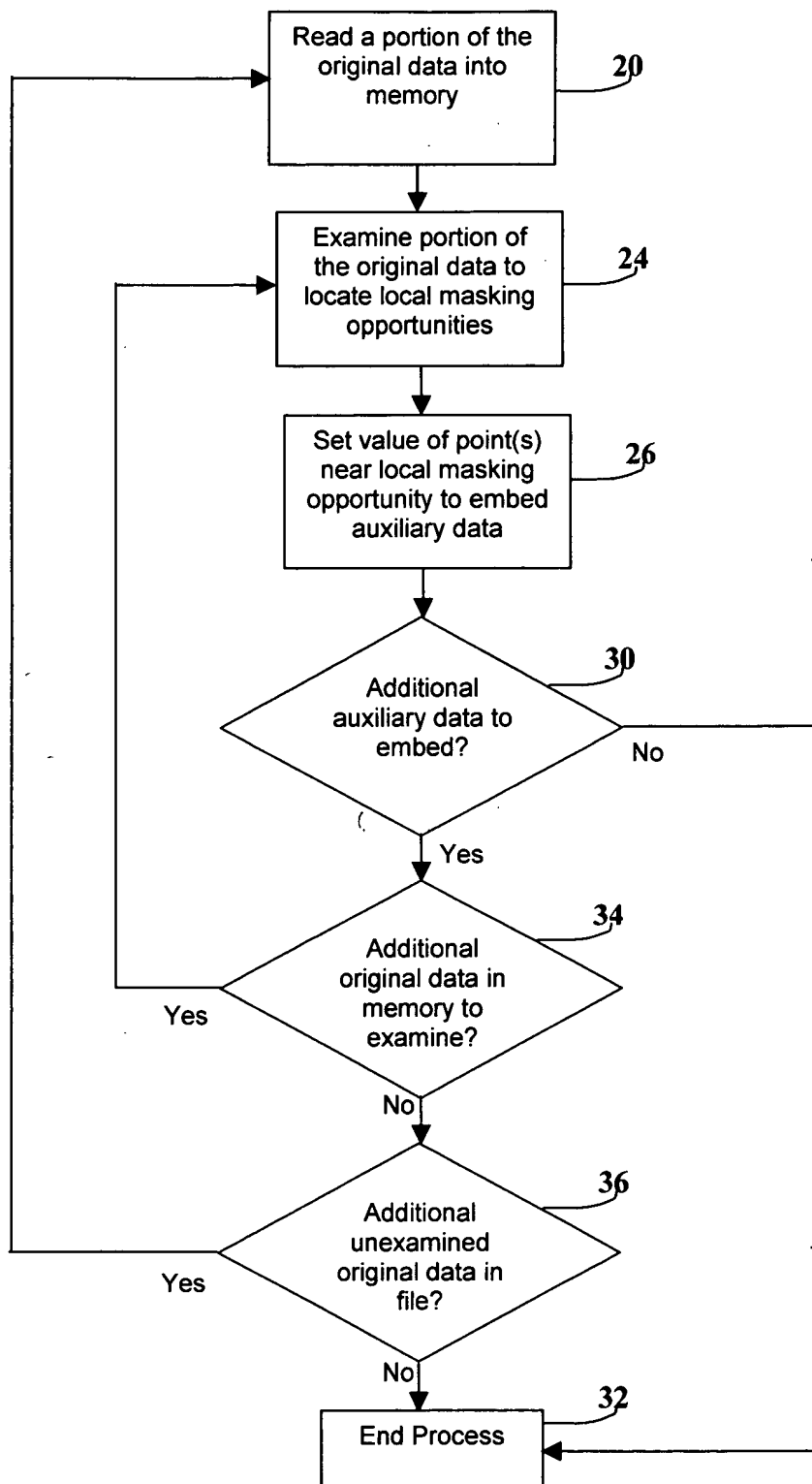


Fig 1

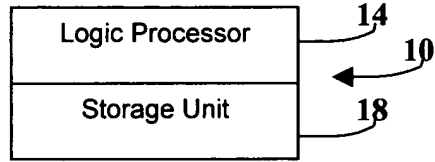


Fig. 2

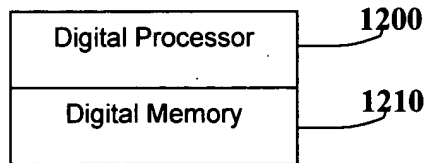


Fig. 12

A to D Converter	Sample and Hold	D to A Converter
Comparator	PLC	Delays

Fig 13

3/9

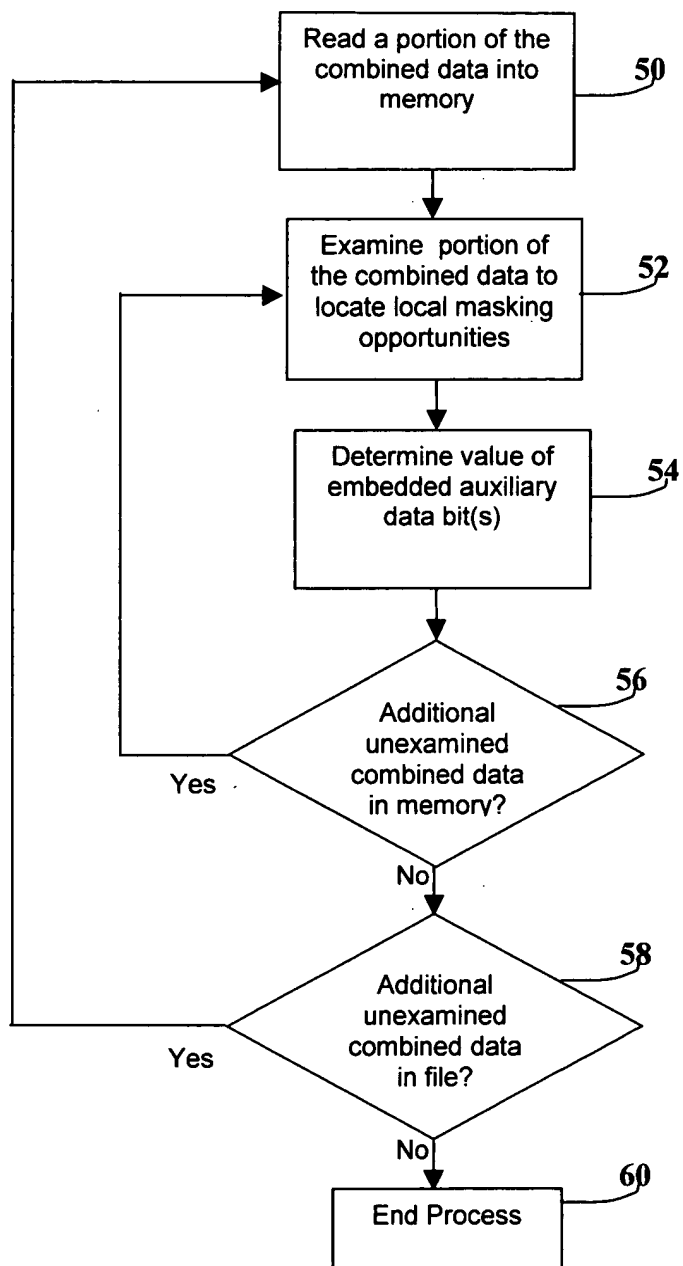


Fig 3

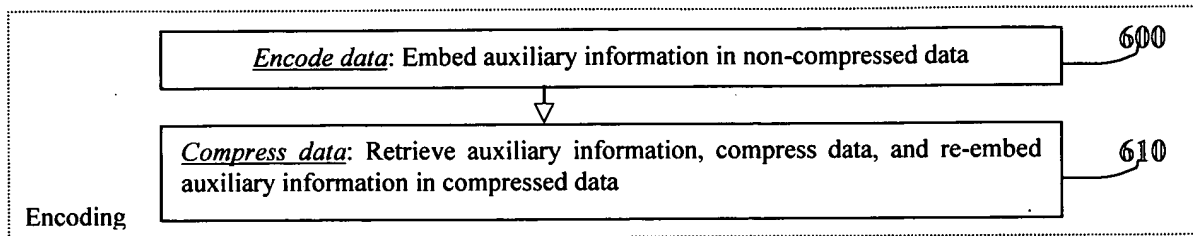


Fig. 10A

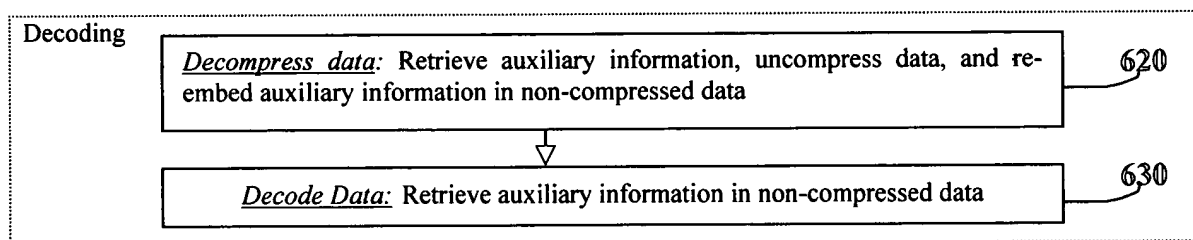


Fig. 10B



Fig. 4

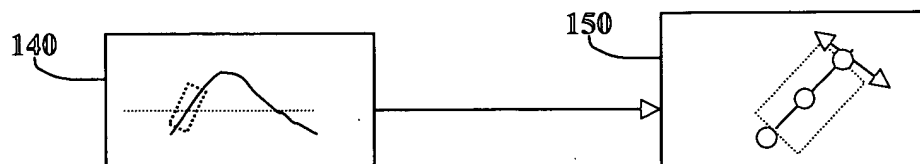


Fig. 7

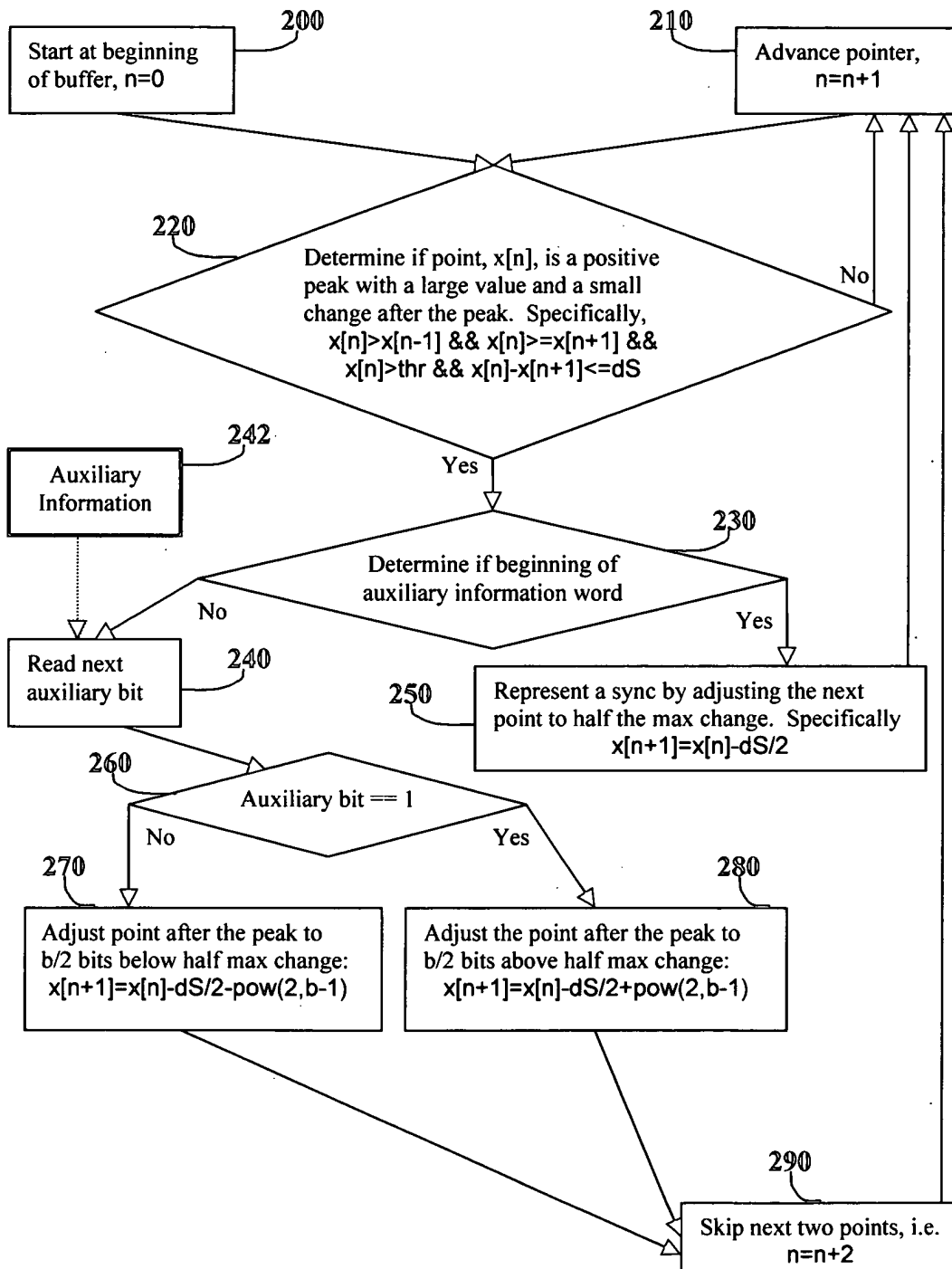


Fig. 5

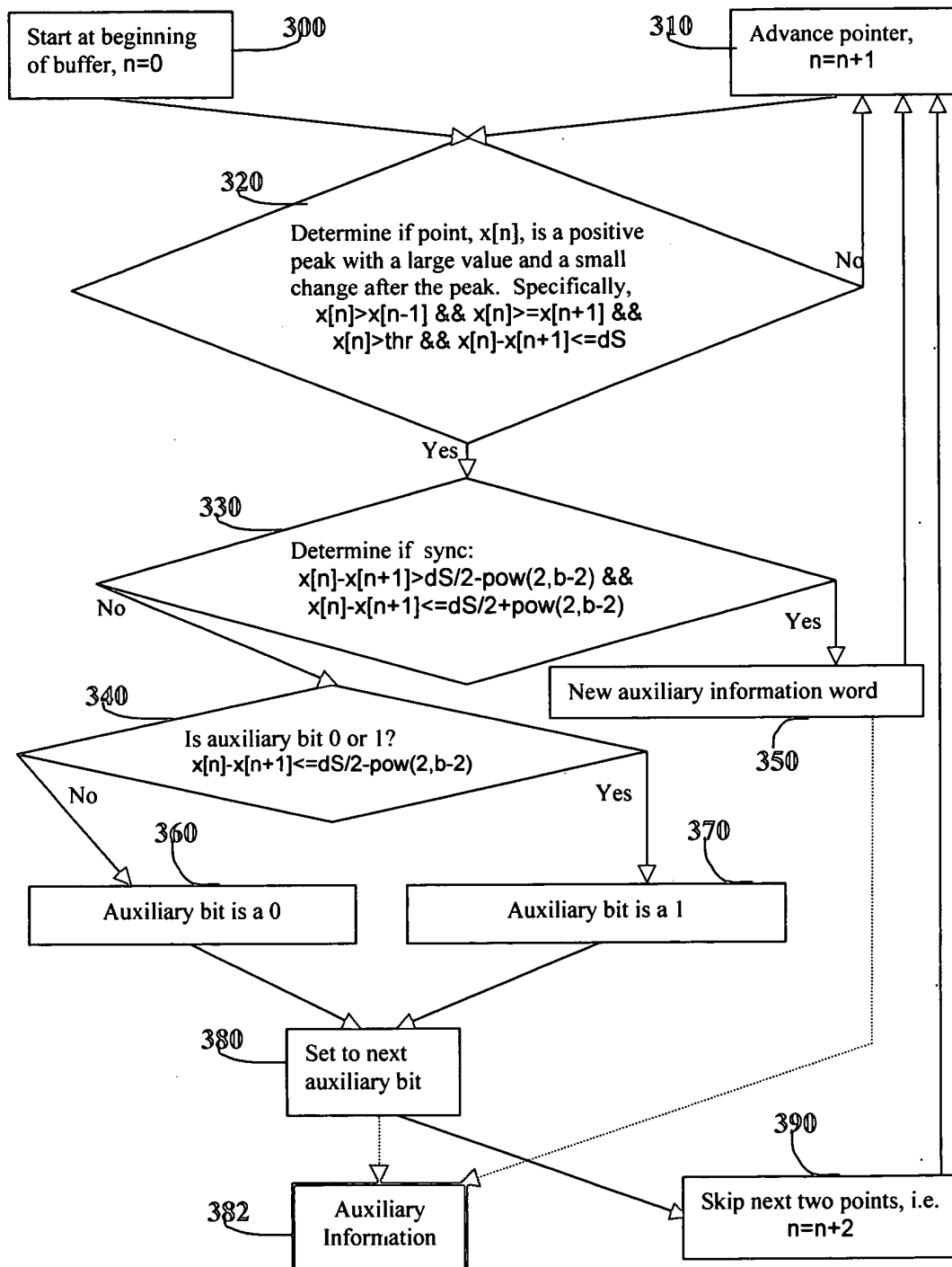


Fig. 6

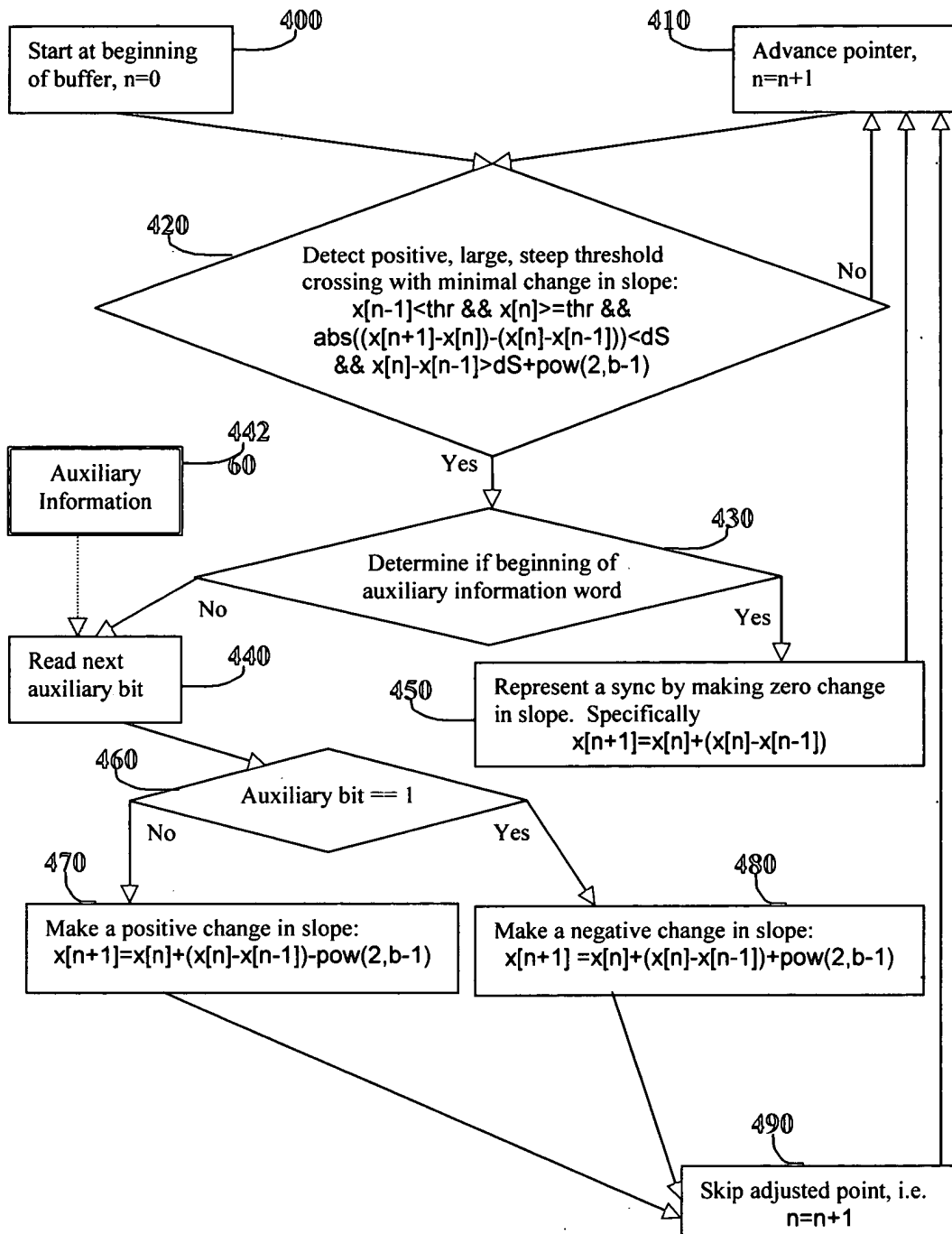


Fig. 8

8/9

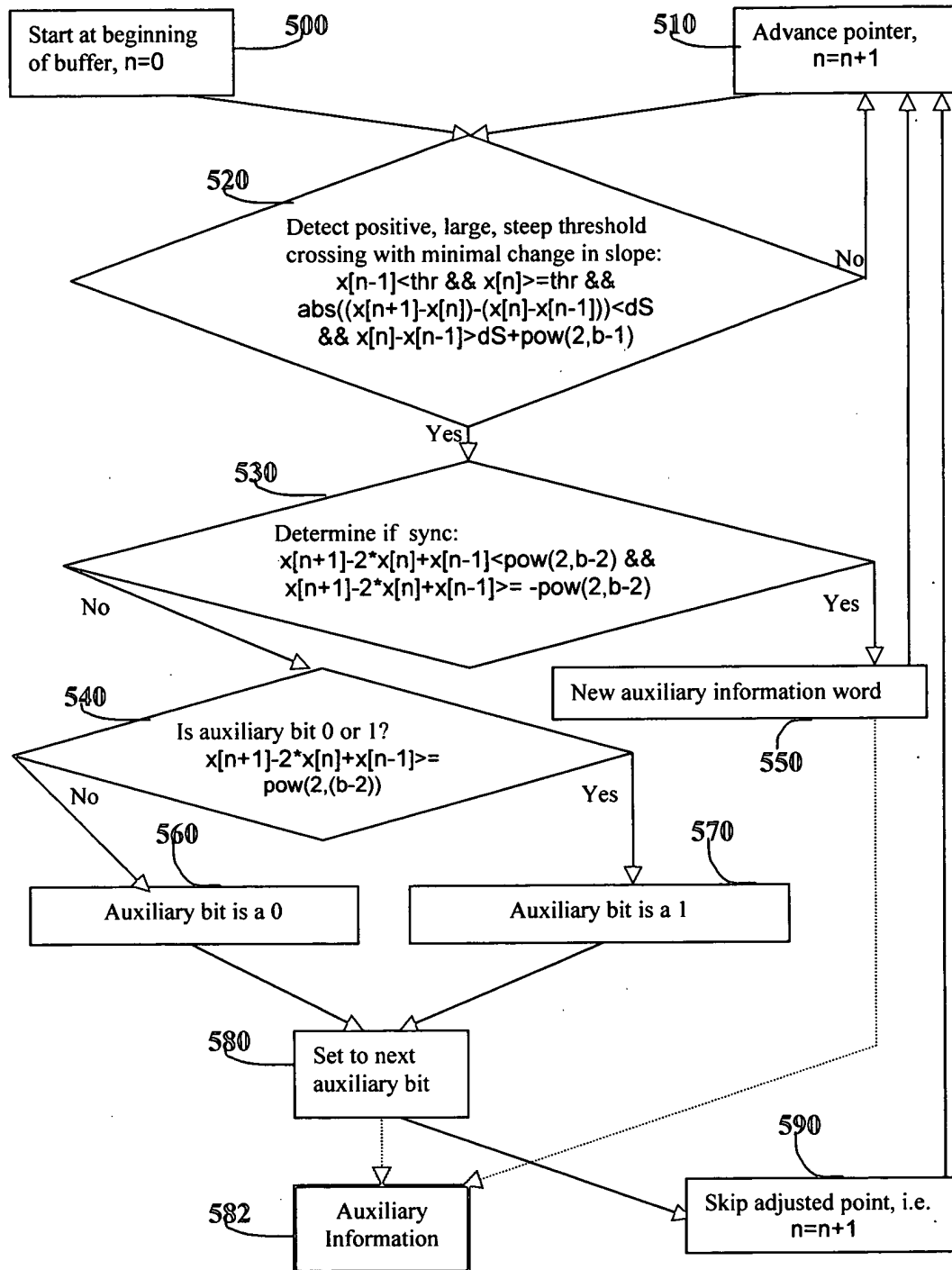


Fig. 9

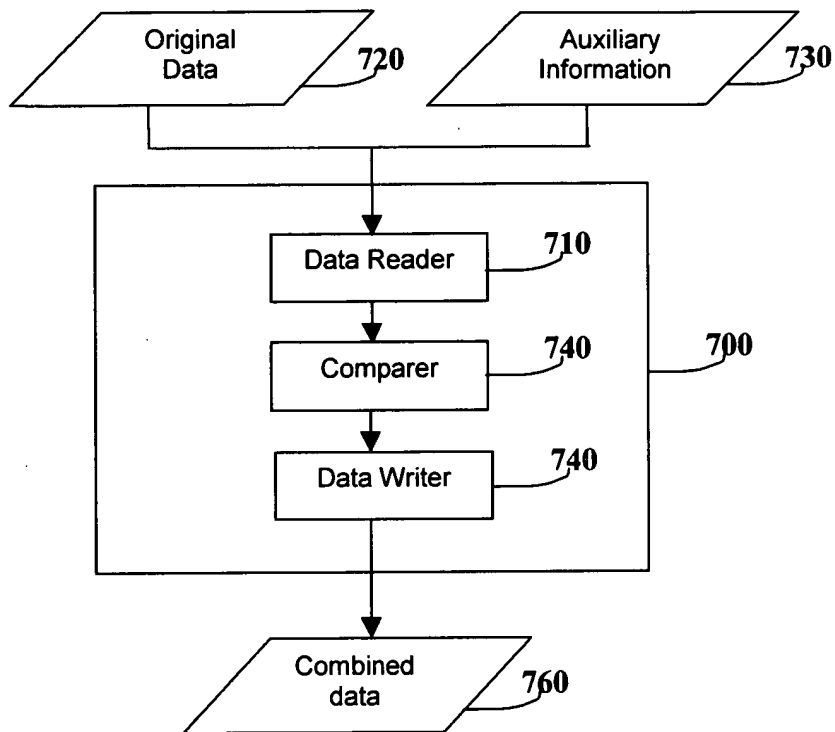


Fig. 11A

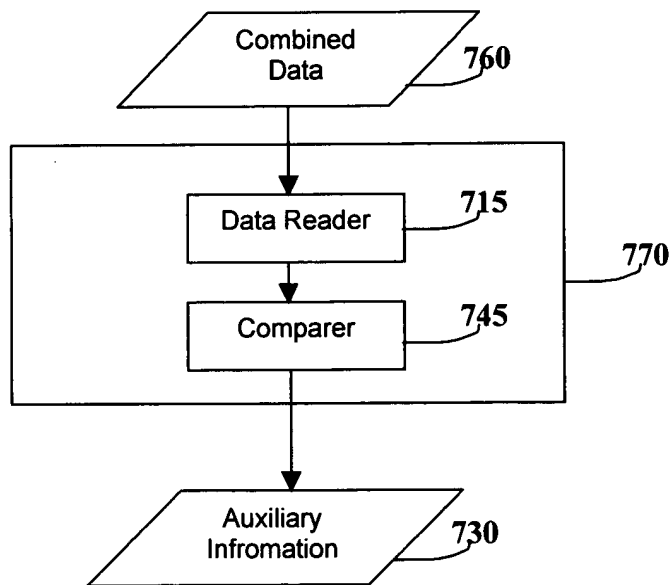


Fig. 11B